CLAIMS

What is claimed is:

1. A non-volatile static random access memory (SRAM) cell, comprising:

an SRAM unit, which receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operations; and

a non-volatile memory unit, which connects to the SRAM unit for storing the 1-bit datum in the SRAM unit before power is turned off (storage operation), keeping the 1-bit datum (storage operation), recovering the 1-bit datum back to the SRAM unit once the power supply is resumed (recovery operation), and erasing the 1-bit after the recovery operation is completed (erase operation).

2. The non-volatile SRAM cell of claim 1, wherein the SRAM unit further comprises a pair of inverters and two n-channel metal oxide semiconductor field effect transistors (nMOSFET's), the gates of the nMOSFET's connecting to a word line.

3. The non-volatile SRAM cell of claim 1, wherein the non-volatile memory unit further comprises two split-gate transistors.

4. The non-volatile SRAM cell of claim 1, wherein the voltage on the control gate of the split-gate transistors is negative and their sources have a high voltage greater than 5V during the erase operation.

5. The non-volatile SRAM cell of claim 1, wherein the voltage on the control gate of the split-gate transistors is 0V and their sources have a voltage selected from 0V and floating.

6. The non-volatile SRAM cell of claim 1, wherein the voltage on the control gate of the split-gate transistors is greater than that of their sources during the storage operation.

7. The non-volatile SRAM cell of claim 1, wherein the voltage on the control gate of the split-gate transistors is equal to that of their sources during the recovery operation.

8. The non-volatile SRAM cell of claim 1, wherein the voltage on the word line of the SRAM unit is pulled down to a low level during the recovery operation, the erase operation, and the storage operation.

9. A non-volatile static random access memory (SRAM) cell, comprising:

an SRAM unit, which comprises a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth transistor, wherein the first transistor and the third transistor form a first inverter, the second transistor and the fourth transistor form a second inverter, the gates of the first transistor and the third transistor are connected to the drains of the fourth transistor and the sixth transistor, the gates of the second transistor and the fourth transistor are connected to the drains of the first transistor, the third transistor, and the fifth transistor, and the gates of the fifth transistor and the sixth transistor are connected with a word line; and

a non-volatile memory unit, which connects to the SRAM unit and comprises a seventh transistor and an eighth transistor, wherein the gates of the seventh transistor and the eighth transistor are connected, the drain of the seventh transistor and the drains of the first transistor, the third transistor, and the fifth transistor are connected, and the eighth transistor is connected to the drains of the second transistor, the fourth transistor, and the sixth transistor;

wherein the SRAM unit receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operations; and the non-volatile memory unit stores the 1-bit datum in the SRAM unit before power is turned off (storage operation), keeps the 1-bit datum (storage operation), recovers the 1-bit datum back to the SRAM unit once the power

supply is resumed (recovery operation), and erases the 1-bit after the recovery operation is completed (erase operation).

10. The non-volatile SRAM cell of claim 9, wherein the first transistor, the second transistor, the fifth transistor, and the sixth transistor are nMOSFET's, and the third transistor and the fourth transistor are pMOSFET's.

11. The non-volatile SRAM cell of claim 9, wherein the seventh transistor and the eighth transistor are split-gate transistors.

12. The non-volatile SRAM cell of claim 9, wherein the voltage on the control gate of the split-gate transistors is negative and their sources have a high voltage greater than 5V during the erase operation.

13. The non-volatile SRAM cell of claim 9, wherein the voltage on the control gate of the split-gate transistors is 0V and their sources have a voltage selected from 0V and floating.

14. The non-volatile SRAM cell of claim 9, wherein the voltage on the control gate of the split-gate transistors is greater than that of their sources during the storage operation.

15. The non-volatile SRAM cell of claim 9, wherein the voltage on the control gate of the split-gate transistors is equal to that of their sources during the recovery operation.

16. The non-volatile SRAM cell of claim 9, wherein the voltage on the word line of the SRAM unit is pulled down to a low level during the recovery operation, the erase operation, and the storage operation.